SSTUB32868

1.8 V 28-bit 1 : 2 configurable registered buffer with parity for DDR2-800 RDIMM applications

Rev. 03 — 7 March 2007 Product data sheet

1. General description

The SSTUB32868 is a 1.8 V 28-bit 1 : 2 register specifically designed for use on two rank by four (2R × 4) and similar high-density Double Data Rate 2 (DDR2) memory modules. It is similar in function to the JEDEC-standard 14-bit DDR2 register, but integrates the functionality of the normally required two registers in a single package, thereby freeing up board real-estate and facilitating routing to accommodate high-density Dual In-line Memory Module (DIMM) designs.

The SSTUB32868 also integrates a parity function, which accepts a parity bit from the memory controller, compares it with the data received on the D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{\text{PTYERR}}$ pin (active LOW).

It further offers added features over the JEDEC standard register in that it can be configured for normal or high output drive strength, simply by tying input pin SELDR either HIGH or LOW as needed. This allows use in different module designs varying from low to high density designs by picking the appropriate drive strength to match net loading conditions. Furthermore, the SSTUB32868 features two additional chip select inputs, which allow more versatile enabling and disabling in densely populated memory modules. Both added features (drive strength and chip selects) are fully backward compatible to the JEDEC standard register.

The SSTUB32868 is packaged in a 176-ball, 8 × 22 grid, 0.65 mm ball pitch, thin profile fine-pitch ball grid array (TFBGA) package, which (while requiring a minimum 6 mm × 15 mm of board space) allows for adequate signal routing and escape using conventional card technology.

2. Features

- 28-bit data register supporting DDR2
- Fully compliant to JEDEC standard for SSTUB32868
- Supports 2 rank by 4 DIMM density by integrating equivalent functionality of two JEDEC-standard DDR2 registers (that is, 2 × SSTUA32864 or 2 × SSTUA32866)
- Parity checking function across 22 input data bits
- Parity out signal
- Controlled multi-impedance output impedance drivers enable optimal signal integrity and speed
- Meets or exceeds SSTUB32868 JEDEC standard speed performance
- Supports up to 450 MHz clock frequency of operation
- Programmable for normal or high output drive
- Optimized pinout for high-density DDR2 module design

- Chip-selects minimize power consumption by gating data outputs from changing state
- Two additional chip select inputs allow optional flexible enabling and disabling
- Supports Stub Series Terminated Logic SSTL_18 data inputs
- Differential clock (CK and $\overline{CK}$) inputs
- Supports Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) switching levels on the control and $\overline{RESET}$ inputs
- Single 1.8 V supply operation (1.7 V to 2.0 V)
- Available in 176-ball 6 mm × 15 mm, 0.65 mm ball pitch TFBGA package

3. Applications

- 400 MT/s to 800 MT/s high-density (for example, 2 rank by 4) DDR2 registered DIMMs
- DDR2 Registered DIMMs (RDIMM) desiring parity checking functionality

4. Ordering information

Table 1. Ordering information

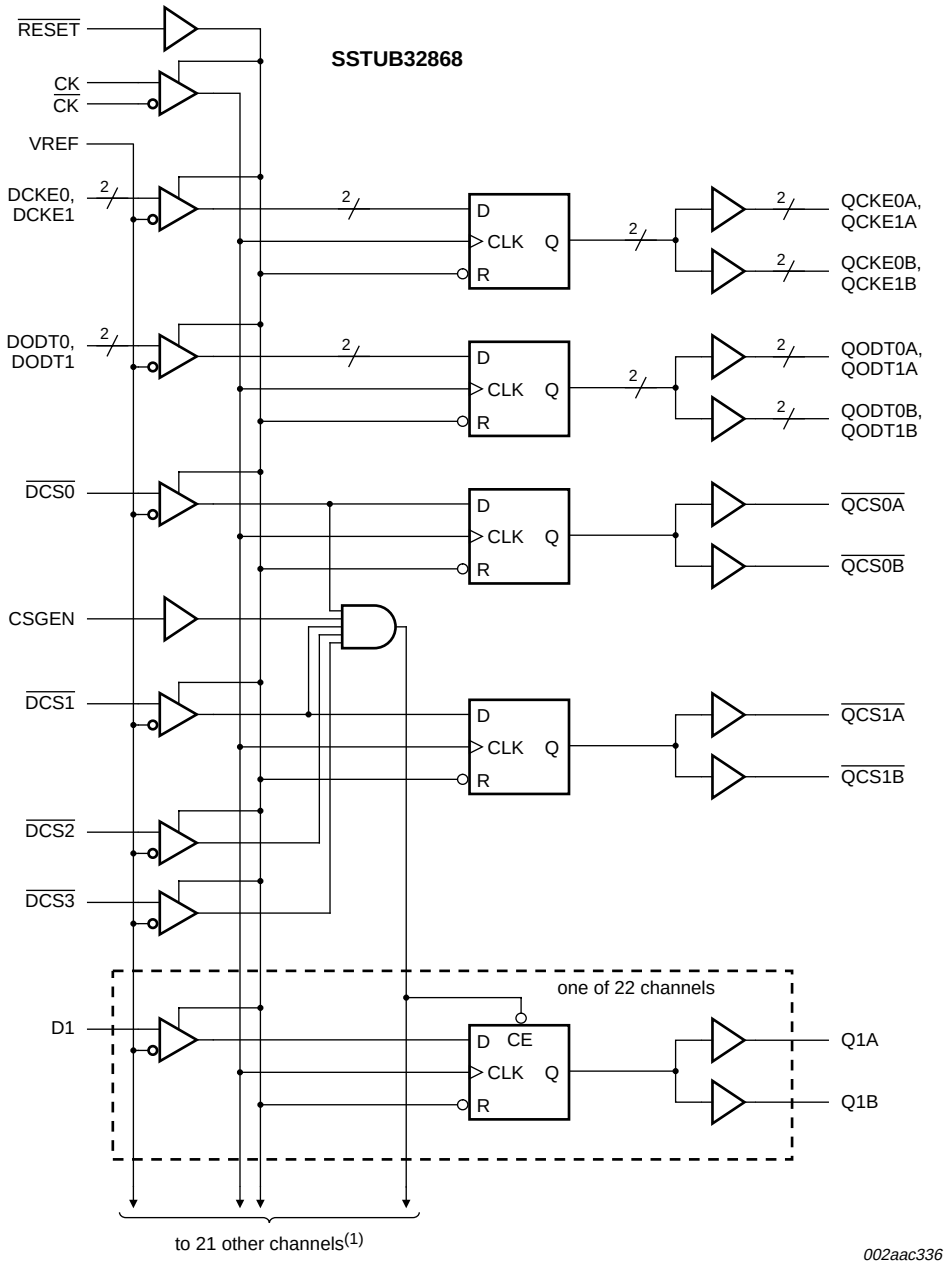
Type number	Solder process	Package		
		Name	Description	Version
SSTUB32868ET/G	Pb-free (SnAgCu solder ball compound)	TFBGA176	plastic thin fine-pitch ball grid array package; 176 balls; body 6 × 15 × 0.7 mm	SOT932-1
SSTUB32868ET/S	Pb-free (SnAgCu solder ball compound)	TFBGA176	plastic thin fine-pitch ball grid array package; 176 balls; body 6 × 15 × 0.7 mm	SOT932-1

4.1 Ordering options

Table 2. Ordering options

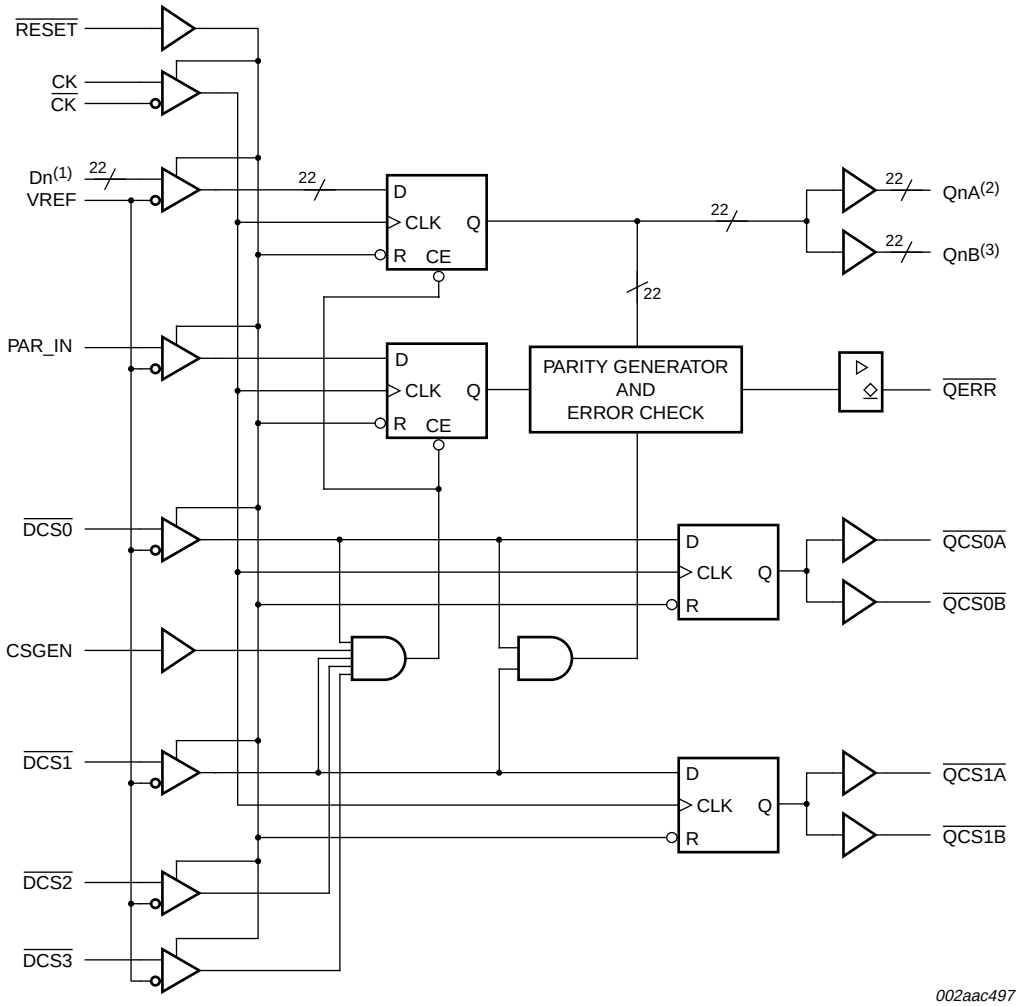
Type number	Temperature range
SSTUB32868ET/G	T_{amb} = 0 °C to +70 °C
SSTUB32868ET/S	T_{amb} = 0 °C to +85 °C

5. Functional diagram



(1) Register A configuration (C = 0): D2 to D5, D7, D9 to D12, D17 to D28
Register B configuration (C = 1): D2 to D12, D17 to D20, D22, D24 to D28

Fig 1. Logic diagram of SSTUB32868 (positive logic)



(1) Register A configuration (C = 0): D1 to D5, D7, D9 to D12, D17 to D28
Register B configuration (C = 1): D1 to D12, D17 to D20, D22, D24 to D28

(2) Register A configuration (C = 0): Q1A to Q5A, Q7A, Q9A to Q12A, Q17A to Q28A
Register B configuration (C = 1): Q1A to Q12A, Q17A to Q20A, Q22A, Q24A to Q28A

(3) Register A configuration (C = 0): Q1B to Q5B, Q7B, Q9B to Q12B, Q17B to Q28B
Register B configuration (C = 1): Q1B to Q12B, Q17B to Q20B, Q22B, Q24B to Q28B

Fig 2. Parity logic diagram (positive logic)

6. Pinning information

6.1 Pinning

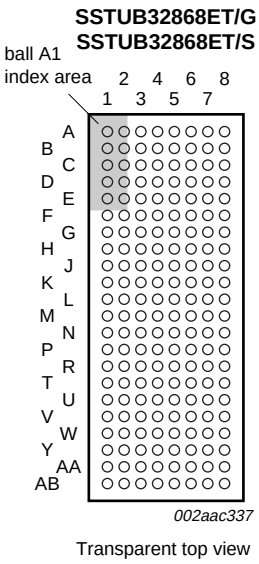


Fig 3. Pin configuration for TFBGA176

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	VREF	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A (QCKE0A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B (QCKE1B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B (QCKE0B)
J	$\overline{\text{DCS1}}$ (D13)	$\overline{\text{QCS1A}}$ (Q13A)	GND	GND	GND	GND	Q10B	Q9B
K	$\overline{\text{DCS0}}$ (D14)	$\overline{\text{QCS0A}}$ (Q14A)	$\overline{\text{DCS2}}$	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B ($\overline{\text{QCS0B}}$)	Q13B ($\overline{\text{QCS1B}}$)
M	$\overline{\text{CK}}$	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$	V_{DD}	V_{DD}	V_{DD}	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (QODT1A)	$\overline{\text{DCS3}}$	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	SELDR	V_{DD}	VREF	V_{DD}	Q28A	Q28B

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176-ball, 8 × 22 grid; top view.

Fig 4. Ball mapping (1 : 2 Register A; C = 0)

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	VREF	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B
J	D13 (DODT1)	Q13A (QODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 (DODT0)	Q14A (QODT0A)	$\overline{DCS2}$	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	$\overline{CK}$	$\overline{RESET}$	QERR	V_{DD}	V_{DD}	V_{DD}	Q15B ($\overline{QCS0B}$)	Q16B ($\overline{QCS1B}$)
N	D15 ($\overline{DCS0}$)	Q15A ($\overline{QCS0A}$)	GND	GND	GND	GND	Q17B	Q18B
P	D16 ($\overline{DCS1}$)	Q16A ($\overline{QCS1A}$)	$\overline{DCS3}$	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	SELDR	V_{DD}	VREF	V_{DD}	Q28A	Q28B

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176-ball, 8 × 22 grid; top view.

Fig 5. Ball mapping (1 : 2 Register B; C = 1)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	1 : 2 Register A (C = 0)	1 : 2 Register B (C = 1)		
Ungated inputs				
DCKE0	D1	W1	SSTL_18	The outputs of this register will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.
DCKE1	C1	Y1		
DODT0	N1	K1	SSTL_18	The outputs of this register will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.
DODT1	P1	J1		
Chip Select gated inputs				
D1 to D28	A2, A1, B2, B1, C2, C1, D2, D1, E1, F1, G1, H1, N1, P1, R1, T1, U1, V1, W1, W2, Y1, Y2, AA1, AA2, AB1, AB2	A2, A1, B2, B1, C2, C1, D2, D1, E1, F1, G1, H1, J1, K1, N1, P1, R1, T1, U1, V1, W1, W2, Y1, Y2, AA1, AA2, AB1, AB2	SSTL_18	Data inputs, clocked in on the crossing of the rising edge of CD and the falling edge of $\overline{CK}$.
Chip Select inputs				
$\overline{DCS0}$	K1	N1	SSTL_18	Chip select inputs. These pins initiate DRAM address/command decodes, and as such at least one will be LOW when a valid address/command is present. The register can be programmed to re-drive all D-inputs (CSGEN = HIGH) only when at least one chip select input is LOW. If CSGEN, $\overline{DCS0}$ and $\overline{DCS1}$ inputs are HIGH, D1 to D28[1] inputs will be disabled.
$\overline{DCS1}$	J1	P1		
$\overline{DCS2}$	K3	K3		
$\overline{DCS3}$	P3	P3		
Configuration control inputs				
C	A3	A3	LVCMOS input	Configuration control inputs; Register A or Register B
Re-driven outputs				
Q1A to Q28A	A7, B7, C7, D7, E7, E2, F7, F2, G7, G2, H7, H2, N2, P2, R2, R7, T2, T7, U2, U7, V2, V7, W7, Y7, AA7, AB7	A7, B7, C7, D7, E7, E2, F7, F2, G7, G2, H7, H2, J2, K2, N2, P2, R2, R7, T2, T7, U2, U7, V2, V7, W7, Y7, AA7, AB7	1.8 V CMOS outputs	Data outputs[2] that are suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.
Q1B to Q28B	A8, B8, C8, D8, E8, F8, G8, H8, J8, J7, K8, K7, L8, L7, M7, M8, N7, N8, P7, P8, R8, T8, V8, U8, W8, Y8, AA8, AB8	A8, B8, C8, D8, E8, F8, G8, H8, J8, J7, K8, K7, L8, L7, M7, M8, N7, N8, P7, P8, R8, T8, U8, V8, W8, Y8, AA8, AB8		
$\overline{QCS0A}$	K2	N2	1.8 V CMOS outputs	Data outputs that will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.
$\overline{QCS0B}$	L7	M7		
$\overline{QCS1A}$	J2	P2		
$\overline{QCS1B}$	L8	M8		

Table 3. Pin description *...continued*

Symbol	Pin		Type	Description
	1 : 2 Register A (C = 0)	1 : 2 Register B (C = 1)		
QCKE0A	F2	U2	1.8 V CMOS outputs	Data outputs that will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.
QCKE0B	H8	R8		
QCKE1A	E2	V2		
QCKE1B	F8	U8		
QODT0A	N2	K2	1.8 V CMOS outputs	Data outputs that will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.
QODT0B	M7	L7		
QODT1A	P2	J2		
QODT1B	M8	L8		
Output error				
$\overline{QERR}$	M3	M3	open-drain output	Output error bit; generated on clock cycle after the corresponding data output.
Parity input				
PAR_IN	L3	L3	SSTL_18	Parity input. Arrives one clock cycle after the corresponding data input.
Program inputs				
CSGEN	L2	L2	LVCMOS input	Chip select gate enable. When HIGH, the D1 to D28[1] inputs will be latched only when at least one chip select input is LOW during the rising edge of the clock. When LOW, the D1 to D28[1] inputs will be latched and re-driven on every rising edge of the clock.
Clock inputs				
CK	L1	L1	differential input	Positive master clock input.
$\overline{CK}$	M1	M1	differential input	Negative master clock input.
Miscellaneous inputs				
$\overline{RESET}$	M2	M2	LVCMOS input	Asynchronous reset input. Resets registers and disables VREF data and clock differential-input receivers.
VREF	A5, AB5	A5, AB5	0.9 V nominal	Input reference voltage.

Table 3. Pin description *...continued*

Symbol	Pin		Type	Description
	1 : 2 Register A (C = 0)	1 : 2 Register B (C = 1)		
V_{DD}	B3, B4, B5, B6, D3, D4, D5, D6, F3, F4, F5, F6, H3, H4, H5, H6, K4, K5, K6, M4, M5, M6, P4, P5, P6, T3, T4, T5, T6, V3, V4, V5, V6, Y3, Y4, Y5, Y6, AB4, AB6	B3, B4, B5, B6, D3, D4, D5, D6, F3, F4, F5, F6, H3, H4, H5, H6, K4, K5, K6, M4, M5, M6, P4, P5, P6, T3, T4, T5, T6, V3, V4, V5, V6, Y3, Y4, Y5, Y6, AB4, AB6	1.8 V nominal	Power supply voltage.
GND	A4, A6, C3, C4, C5, C6, E3, E4, E5, E6, G3, G4, G5, G6, J3, J4, J5, J6, L4, L5, L6, N3, N4, N5, N6, R3, R4, R5, R6, U3, U4, U5, U6, W3, W4, W5, W6, AA3, AA4, AA5, AA6	A4, A6, C3, C4, C5, C6, E3, E4, E5, E6, G3, G4, G5, G6, J3, J4, J5, J6, L4, L5, L6, N3, N4, N5, N6, R3, R4, R5, R6, U3, U4, U5, U6, W3, W4, W5, W6, AA3, AA4, AA5, AA6	ground input	Ground.
SELDR	AB3	AB3	LVCMOS input with weak pull-up	Selects output drive strength: 'HIGH' for normal drive; 'LOW' for high drive. This pin will default HIGH if left open-circuit (built-in weak pull-up resistor).

[1] Data inputs = D1 to D5, D7, D9 to D12, D17 to D28 when C = 0.
Data inputs = D1 to D12, D17 to D20, D22, D24 to D28 when C = 1.

[2] Data outputs = Q1x to Q5x, Q7x, Q9x to Q12x, Q17x to Q28x when C = 0.
Data outputs = Q1x to Q12x, Q17x to Q20x, Q22x, Q24x to Q28x when C = 1.

7. Functional description

7.1 Function table

Table 4. Function table (each flip-flop)

Inputs							Outputs[1]			
$\overline{RESET}$	$\overline{DCS0}$[2]	$\overline{DCS1}$[2]	CSGEN	CK	$\overline{CK}$	Dn, DODTn, DCKEn	Qn	$\overline{QCS0x}$	$\overline{QCS1x}$	QODTn, QCKEn
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L

Table 4. Function table (each flip-flop) *…continued*

Inputs							Outputs[1]			
$\overline{RESET}$	$\overline{DCS0}$[2]	$\overline{DCS1}$[2]	CSGEN	CK	$\overline{CK}$	Dn, DODTn, DCKEn	Qn	$\overline{QCS0x}$	$\overline{QCS1x}$	QODTn, QCKEn
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

[1] Q_0 is the previous state of the associated output.

[2] $\overline{DCS2}$ and $\overline{DCS3}$ operate identically to $\overline{DCS0}$ and $\overline{DCS1}$, except they do not have corresponding re-driven (QCS) outputs.

Table 5. Parity and standby function table

Inputs							Output
$\overline{RESET}$	$\overline{DCS0}$[1]	$\overline{DCS1}$[1]	CK	$\overline{CK}$	∑ of inputs = H (D1 to D28)	PAR_IN[2]	$\overline{QERR}$[3][4]
H	L	X	↑	↓	even	L	H
H	L	X	↑	↓	odd	L	L
H	L	X	↑	↓	even	H	L
H	L	X	↑	↓	odd	H	H
H	X	L	↑	↓	even	L	H
H	X	L	↑	↓	odd	L	L
H	X	L	↑	↓	even	H	L
H	X	L	↑	↓	odd	H	H
H	H	H	↑	↓	X	X	$\overline{QERR}_0$[5]
H	X	X	L or H	L or H	X	X	$\overline{QERR}_0$
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	H

[1] $\overline{DCS2}$ and $\overline{DCS3}$ operate identically to $\overline{DCS0}$ and $\overline{DCS1}$ with regard to the parity function.

[2] PAR_IN arrives one clock cycle after the data to which it applies.

[3] This transition assumes $\overline{QERR}$ is HIGH at the crossing of CK going HIGH and $\overline{CK}$ going LOW. If $\overline{QERR}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{RESET}$ is driven LOW.

[4] $\overline{QERR}_0$ is the previous state of output $\overline{QERR}$.

[5] If $\overline{DCS0}$, $\overline{DCS1}$, $\overline{DCS2}$, $\overline{DCS3}$ and CSGEN are driven HIGH, the device is placed in Low-Power Mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{QERR}$ output is driven LOW, it stays latched LOW for the LPM duration plus two clock cycles or until $\overline{RESET}$ is driven LOW.

7.2 Functional information

The SSTUB32868 is a 28-bit 1 : 2 configurable registered buffer designed for 1.7 V to 1.9 V V_{DD} operation.

All inputs are compatible with the JEDEC standard for SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset ($\overline{RESET}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{QERR}$) output.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is LOW, all registers are reset and all outputs are forced LOW except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and C inputs always must be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the LOW state during power-up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register will be cleared and the data outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTUB32868 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

The SSTUB32868 includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. The corresponding $\overline{\text{QERR}}$ output signal for the data inputs is generated two clock cycles after the data, to which the $\overline{\text{QERR}}$ signal applies, is registered.

The SSTUB32868 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D inputs (D1 to D5, D7, D9 to D12, D17 to D28 when C = 0; or D1 to D12, D17 to D20, D22, D24 to D28 when C = 1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active LOW). The convention is even parity, that is, valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D inputs must be tied to a known logic state.

If an error occurs and the $\overline{\text{QERR}}$ output is driven LOW, it stays latched LOW for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven LOW. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven LOW and latched LOW for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven LOW. If a parity error occurs on the clock cycle before the device enters the Low-Power Mode (LPM) and the $\overline{\text{QERR}}$ output is driven LOW, then it stays latched LOW for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven LOW. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$) are not included in the parity check computation.

The C input controls the pinout configuration from Register A configuration (when LOW) to Register B configuration (when HIGH). The C input should not be switched during normal operation. It should be hard-wired to a valid LOW or HIGH level to configure the register in the desired mode.

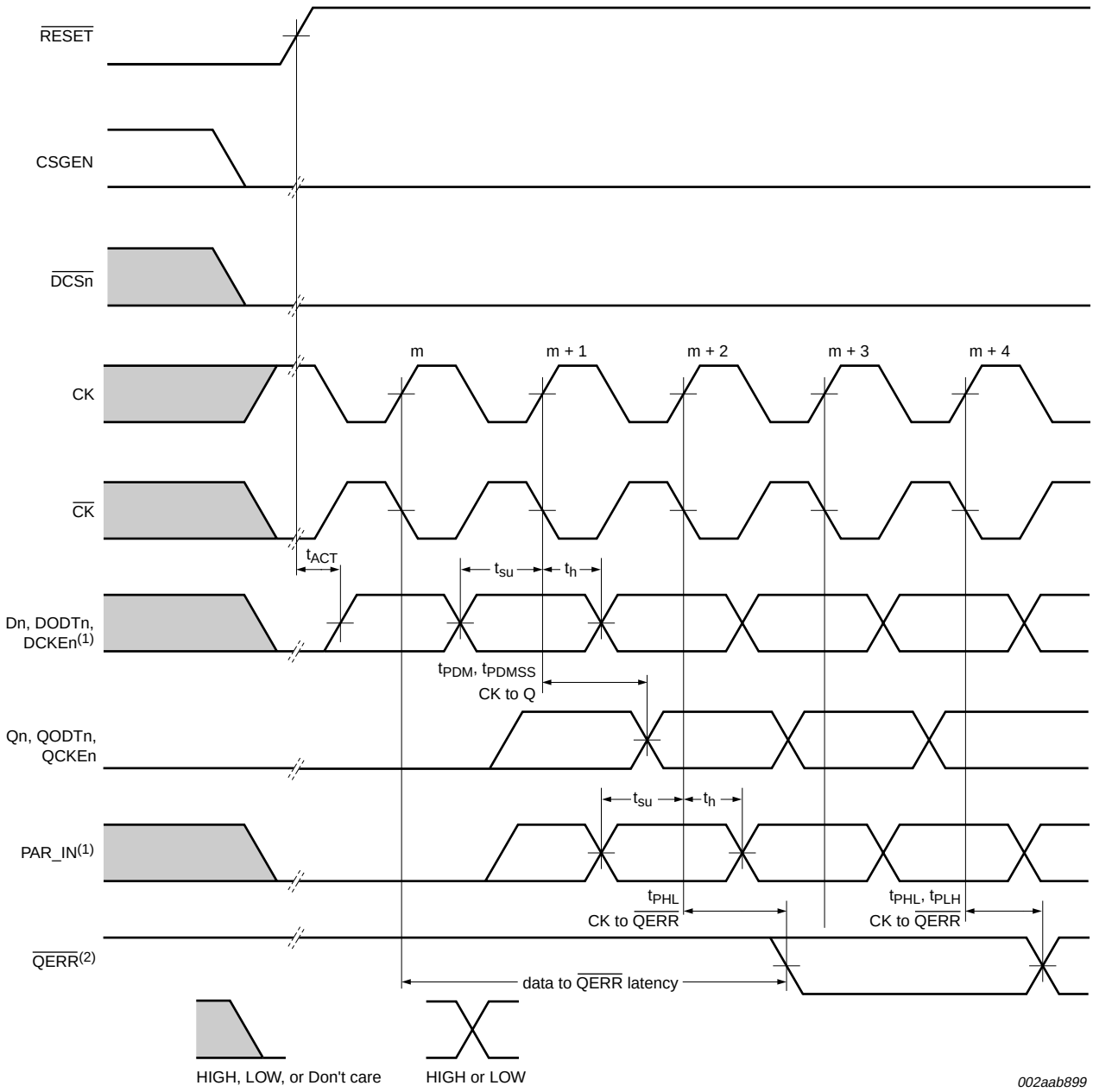
The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs are HIGH. If CSGEN or the $\overline{\text{DCSn}}$ inputs are LOW, the Qn outputs will function normally. Also, if all $\overline{\text{DCSn}}$ inputs are HIGH, the device will gate the $\overline{\text{QERR}}$ output from changing states. If any of the $\overline{\text{DCSn}}$ are

LOW, the $\overline{QERR}$ output will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCSn}$ control, and when driven LOW will force the Qn outputs LOW and the $\overline{QERR}$ output HIGH. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground (GND), in which case the setup time requirement for $\overline{DCSn}$ would be the same as for the other D data inputs. To control the Low-power mode with $\overline{DCSn}$ only, the CSGEN input should be pulled up to V_{DD} through a pull-up resistor.

The two VREF pins (A5 and AB5) are connected together internally by approximately 150 Ω. However, it is necessary to connect only one of the two VREF pins to the external V_{ref} power supply. An unused VREF pin should be terminated with a V_{ref} coupling capacitor.

The SSTUB32868 is available in a TFGBA176 package.

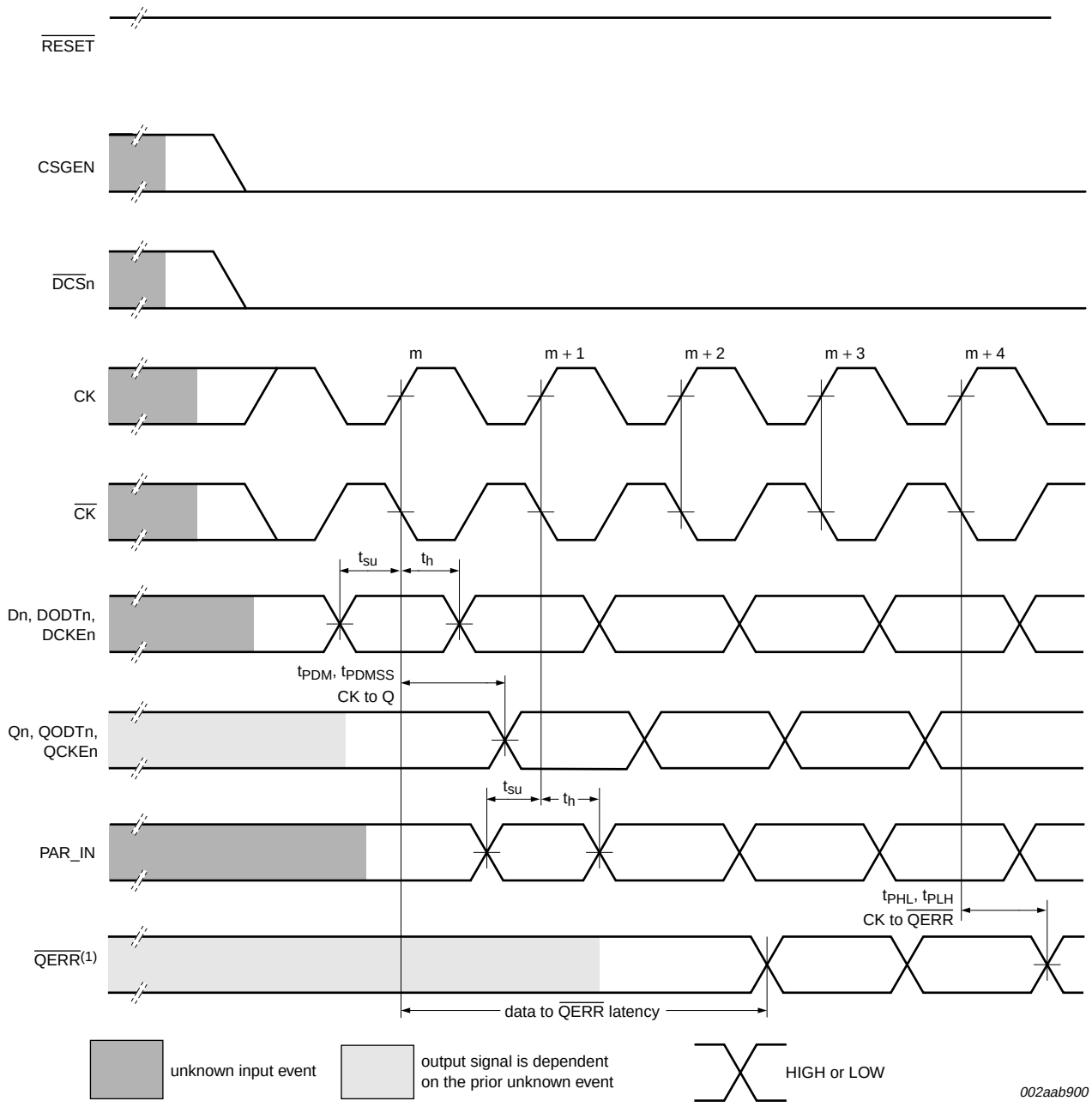
7.3 Register timing



(1) After $\overline{\text{RESET}}$ is switched from LOW to HIGH, all data and PAR_IN input signals must be set and held LOW for a minimum time of $t_{ACT(max)}$ to avoid false error.

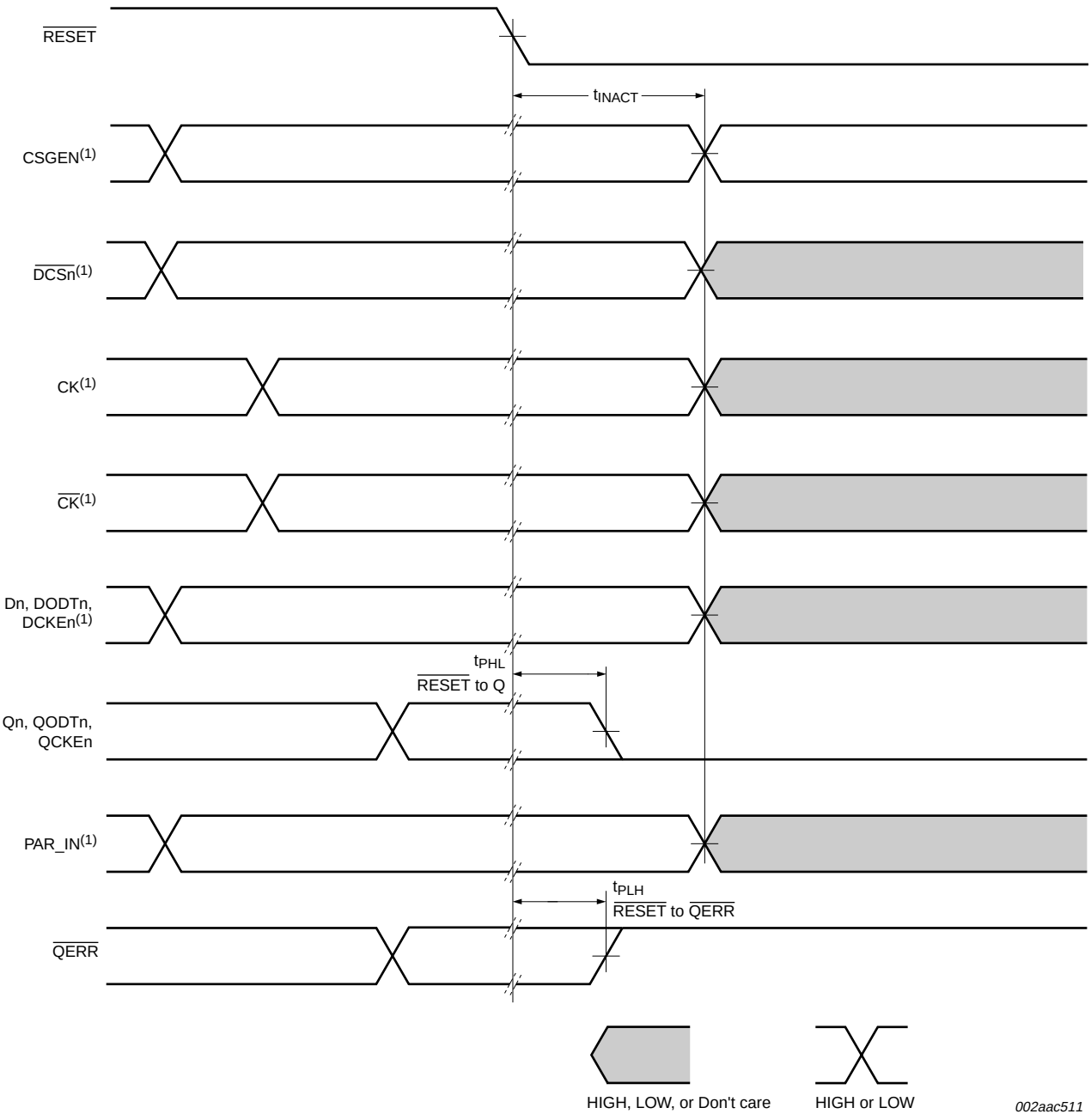
(2) If the data is clocked on the m clock pulse, and PAR_IN is clocked in at m + 1, the $\overline{\text{QERR}}$ output signal will be produced on the m + 2 clock pulse and it will be valid on the m + 3 clock pulse.

Fig 6. Timing diagram during start-up ($\overline{\text{RESET}}$ switches from LOW to HIGH)



(1) If the data is clocked in on the m clock pulse, and PAR_IN is clocked in at m + 1, the $\overline{QERR}$ output signal will be generated on the m + 2 clock pulse and it will be valid on the m + 3 clock pulse. If an error occurs and the $\overline{QERR}$ output is driven LOW, it stays LOW for a minimum of two clock cycles or until $\overline{RESET}$ is driven LOW.

Fig 7. Timing diagram during normal operation ($\overline{RESET}$ = HIGH)



(1) After $\overline{\text{RESET}}$ is switched from HIGH to LOW, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of $t_{INACT(max)}$.

Fig 8. Timing diagram during shutdown ($\overline{\text{RESET}}$ switches from HIGH to LOW)

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+2.5	V
V_I	input voltage (receiver)		[1][2]	–0.5	+2.5	V
V_O	output voltage (driver)		[1][2]	–0.5	V_{DD} + 0.5	V
I_{IK}	input clamping current	$V_I < 0$ V or $V_I > V_{DD}$		-	±50	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{DD}$		-	±50	mA
I_O	output current (continuous)	$0 V < V_O < V_{DD}$		-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); 1.5 kΩ; 100 pF		2	-	kV
		Machine Model (MM); 0 Ω; 200 pF		200	-	V

[1] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

[2] This value is limited to 2.5 V maximum.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	2.0	V
V_{ref}	reference voltage			$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_T	termination voltage			V_{ref} – 0.040	V_{ref}	V_{ref} + 0.040	V
V_I	input voltage			0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	Dn, $\overline{CSR}$ and PAR_IN inputs	[1]	V_{ref} + 0.250	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	Dn, $\overline{CSR}$ and PAR_IN inputs	[1]	-	-	V_{ref} – 0.250	V
$V_{IH(DC)}$	DC HIGH-level input voltage	Dn, $\overline{CSR}$ and PAR_IN inputs	[1]	V_{ref} + 0.125	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	Dn, $\overline{CSR}$ and PAR_IN inputs	[1]	-	-	V_{ref} – 0.125	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, CSGEN	[2]	$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$, CSGEN	[2]	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	CK, $\overline{CK}$		0.675	-	1.125	V
V_{ID}	differential input voltage	CK, $\overline{CK}$		600	-	-	mV
I_{OH}	HIGH-level output current	SELDR either HIGH or LOW		-	-	–8	mA
I_{OL}	LOW-level output current	SELDR either HIGH or LOW		-	-	8	mA
T_{amb}	ambient temperature	operating in free air					
		SSTUB32868ET/G		0	-	70	°C
		SSTUB32868ET/S		0	-	85	°C

[1] The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

[2] The $\overline{RESET}$ input of the device must be held at valid logic levels (not floating) to ensure proper device operation.

10. Characteristics

Table 8. Characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = –6 mA; V_{DD} = 1.7 V	1.2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA; V_{DD} = 1.7 V	-	-	0.5	V
I_I	input current	all inputs; $V_I = V_{DD}$ or GND; V_{DD} = 1.9 V	-	-	±5	µA
I_{DD}	supply current	static standby; $\overline{RESET}$ = GND; V_{DD} = 1.9 V; I_O = 0 mA	-	-	2	mA
		static operating; $\overline{RESET} = V_{DD}$; V_{DD} = 1.9 V; I_O = 0 mA; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	80	mA
I_{DDD}	dynamic operating current per MHz	clock only; $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. I_O = 0 mA; V_{DD} = 1.8 V	-	16	-	µA
		per each data input (1 : 1 mode); $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle; one data input switching at half clock frequency, 50 % duty cycle; I_O = 0 mA; V_{DD} = 1.8 V	-	19	-	µA
		per each data input (1 : 2 mode); $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle; one data input switching at half clock frequency, 50 % duty cycle; I_O = 0 mA; V_{DD} = 1.8 V	-	19	-	µA
C_i	input capacitance	Dn, CSGEN, PAR_IN inputs; $V_I = V_{ref} \pm 250$ mV; V_{DD} = 1.8 V	2.5	-	4	pF
		$\overline{DCSn}$; V_{ICR} = 0.9 V; V_{ID} = 600 mV; V_{DD} = 1.8 V	2.5	-	4	pF
		CK and $\overline{CK}$; V_{ICR} = 0.9 V; V_{ID} = 600 mV; V_{DD} = 1.8 V	2	-	3	pF
		$\overline{RESET}$; $V_I = V_{DD}$ or GND; V_{DD} = 1.8 V	3	-	5	pF
Z_o	output impedance	normal drive; instantaneous [1]	-	15	-	Ω
		normal drive; steady-state	-	53	-	Ω
		high drive; instantaneous [1]	-	7	-	Ω
		high drive; steady-state	-	53	-	Ω

[1] Instantaneous is defined as within < 2 ns following the output data transition edge.

Table 9. Timing requirements

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			-	-	450	MHz
t_W	pulse duration	CK, $\overline{CK}$ HIGH or LOW		1	-	-	ns
t_{ACT}	differential inputs active time		[1][2]	-	-	10	ns
t_{INACT}	differential inputs inactive time		[1][3]	-	-	15	ns
t_{su}	setup time	$\overline{DCSn}$ before CK↑, $\overline{CK}$↓, $\overline{CSR}$ HIGH; $\overline{CSR}$ before CK↑, $\overline{CK}$↓, $\overline{DCSn}$ HIGH		0.6	-	-	ns
		$\overline{DCSn}$ before CK↑, $\overline{CK}$↓, $\overline{CSR}$ LOW		0.5	-	-	ns
		DODTn, DCKEn ad Dn before CK↑, $\overline{CK}$↓		0.5	-	-	ns
		PAR_IN before CK↑, $\overline{CK}$↓		0.5	-	-	ns
t_h	hold time	$\overline{DCSn}$, DODTn, DCKEn and Dn after CK↑, $\overline{CK}$↓		0.4	-	-	ns
		PAR_IN after CK↑, $\overline{CK}$↓		0.4	-	-	ns

[1] This parameter is not necessarily production tested.

[2] VREF must be held at a valid input voltage level, and data inputs must be held LOW for a minimum time of $t_{ACT(max)}$ after $\overline{RESET}$ is taken HIGH.

[3] VREF, data and clock inputs must be held at valid voltage levels (not floating) a minimum time of $t_{INACT(max)}$ after $\overline{RESET}$ is taken LOW.

Table 10. Switching characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	input		450	-	-	MHz
t_{PDM}	peak propagation delay	single bit switching; from CK↑ and $\overline{CK}$↓ to Qn	[1]	1.1	-	1.5	ns
t_{PLH}	LOW-to-HIGH propagation delay	from CK↑ and $\overline{CK}$↓ to $\overline{QERR}$		1.2	-	3	ns
		from $\overline{RESET}$↑ to $\overline{QERR}$↓		-	-	3	ns
t_{PHL}	HIGH-to-LOW propagation delay	from CK↑ and $\overline{CK}$↓ to $\overline{QERR}$		1	-	2.4	ns
		from $\overline{RESET}$↑ to Qn↓		-	-	3	ns
t_{PDMSS}	simultaneous switching peak propagation delay	from CK↑ and $\overline{CK}$↓ to Qn	[1]	-	-	1.6	ns

[1] Includes 350 ps of test-load transmission line delay.

Table 11. Output edge rates

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt_r	rising edge slew rate	from 20 % to 80 %	1	-	4	V/ns
dV/dt_f	falling edge slew rate	from 80 % to 20 %	1	-	4	V/ns
dV/dt_Δ	absolute difference between dV/dt_r and dV/dt_f	(from 20 % to 80 %) or (from 80 % to 20 %)	-	-	1	V/ns

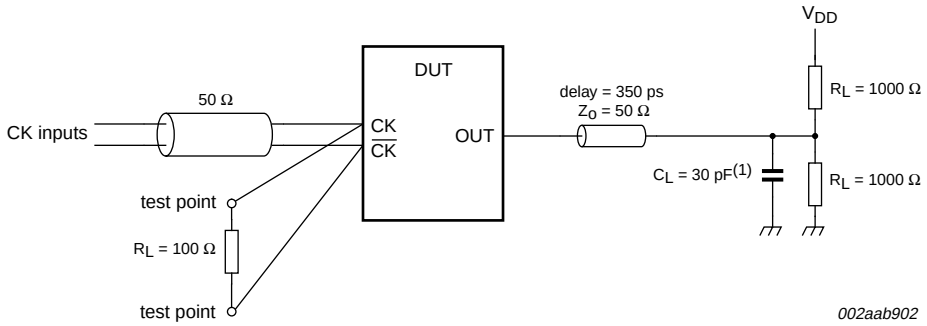
11. Test information

11.1 Parameter measurement information for data output load circuit

V_{DD} = 1.8 V ± 0.1 V.

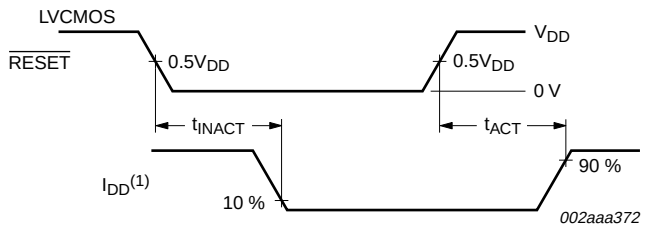
All input pulses are supplied by generators having the following characteristics: Pulse Repetition Rate (PRR) ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



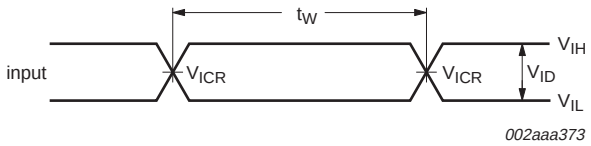
(1) C_L includes probe and jig capacitance.

Fig 9. Load circuit, data output measurements



(1) I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Fig 10. Voltage and current waveforms; inputs active and inactive times

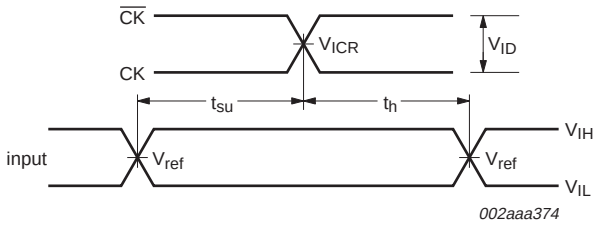


V_{ID} = 600 mV.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 11. Voltage waveforms; pulse duration



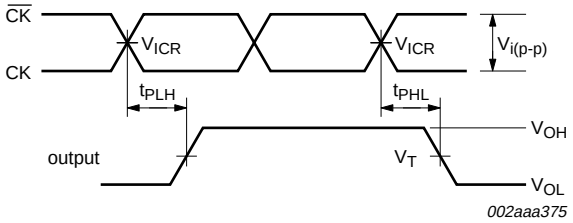
V_{ID} = 600 mV.

$V_{ref} = 0.5V_{DD}$.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

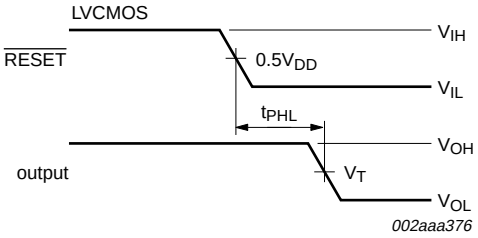
$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 12. Voltage waveforms; setup and hold times



t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig 13. Voltage waveforms; propagation delay times (clock to output)



t_{PLH} and t_{PHL} are the same as t_{PD}.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

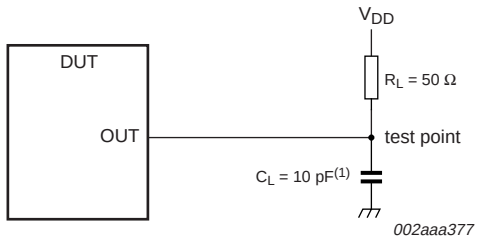
$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 14. Voltage waveforms; propagation delay times (reset to output)

11.2 Data output slew rate measurement

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 15. Load circuit, HIGH-to-LOW slew measurement

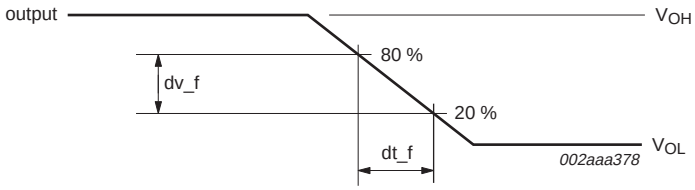
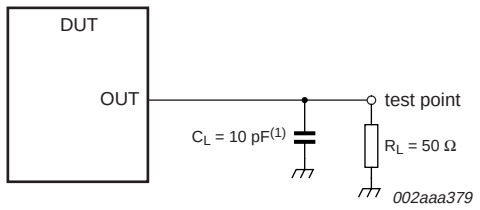


Fig 16. Voltage waveforms, HIGH-to-LOW slew rate measurement



(1) C_L includes probe and jig capacitance.

Fig 17. Load circuit, LOW-to-HIGH slew measurement

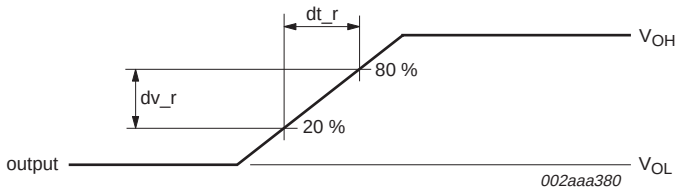
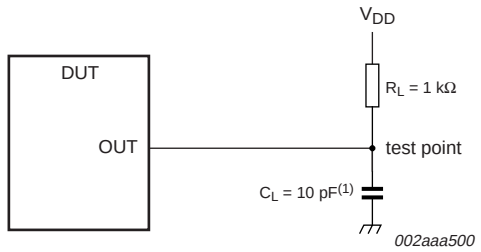


Fig 18. Voltage waveforms, LOW-to-HIGH slew rate measurement

11.3 Error output load circuit and voltage measurement

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 19. Load circuit, error output measurements

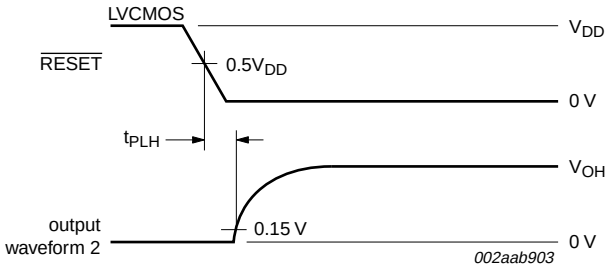


Fig 20. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to $\overline{\text{RESET}}$ input

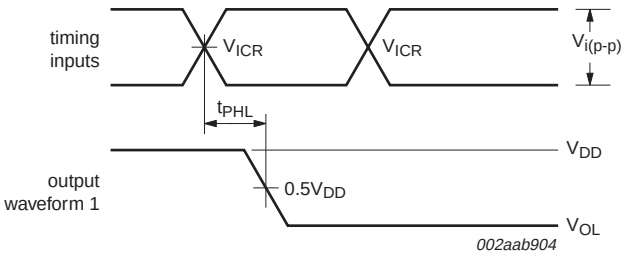


Fig 21. Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs

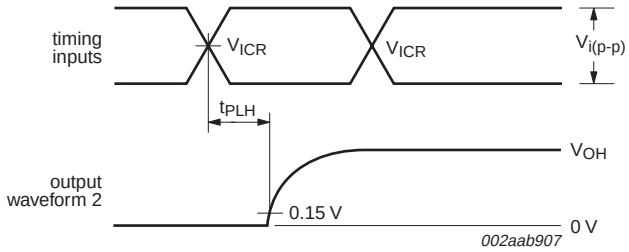
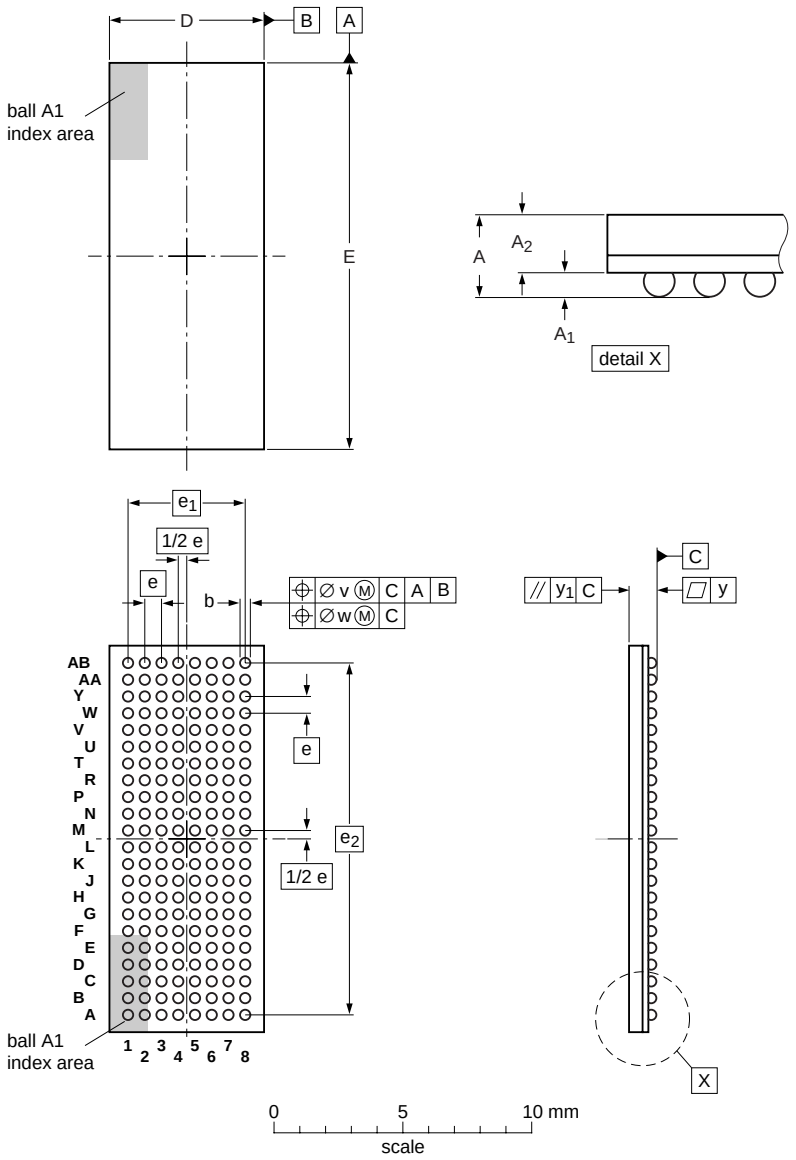


Fig 22. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs

12. Package outline

TFBGA176: plastic thin fine-pitch ball grid array package; 176 balls; body 6 x 15 x 0.7 mm **SOT932-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.35 0.25	0.80 0.65	0.45 0.35	6.1 5.9	15.1 14.9	0.65	4.55	13.65	0.15	0.08	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT932-1	- - -	MO-246	- - -			~~06-01-11~~ 06-01-16

Fig 23. Package outline SOT932-1 (TFBGA176)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

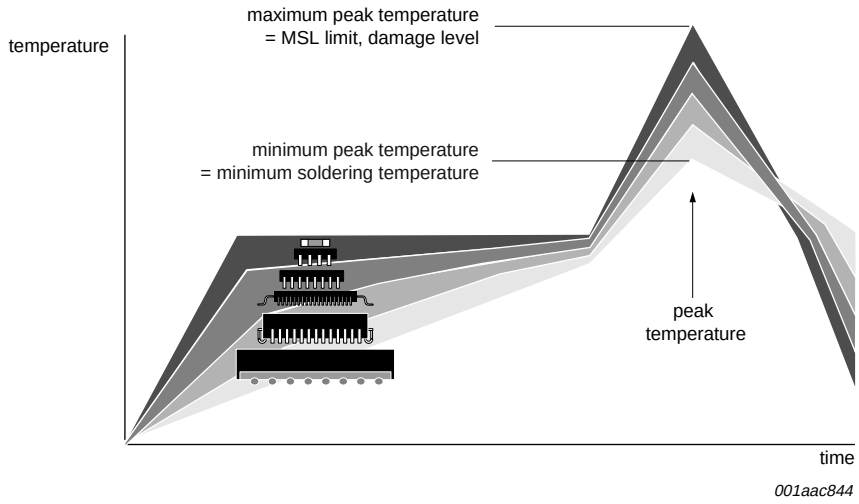
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DDR2	Double Data Rate 2
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
RDIMM	Registered Dual In-line Memory Module
SSTL	Stub Series Terminated Logic

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSTUB32868_3	20070307	Product data sheet	-	SSTUB32868_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 8 "Characteristics", I_{DD}, static standby (Max) changed from "100 µA" to "2 mA"			
SSTUB32868_2	20060912	Product data sheet	-	SSTUB32868_1
SSTUB32868_1	20060825	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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